

Notice of References Cited

Application/Control No.

09/411,434

Applicant(s)/Patent Under
Reexamination
TARDIEUX, JEAN-LOUIS

Examiner

Stephanie M. Deckter

Art Unit

2183

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,073,855	12-1991	Staplin et al.	712/217
	B	US-5,333,176	07-1994	Burke et al.	455/412
	C	US-			
	D	US-			
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	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Nelson, Victor P. et al., Digital Logic Circuit Analysis & Design, 1995, Prentice-Hall, Inc., Pages 173-196
	V	Smith, J.E. and G.S. Sohi, The Microarchitecture of Superscalar Processors, December 1995, Proceedings of the IEEE, Vol. 83, No. 12, Pages 1609-1624
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	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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